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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,185	03/06/2002	Raymond J. Beffa	3037.10US (95-1074.10)	1655
24247	7590	03/31/2005	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			RODRIGUEZ, JOSEPH C	
			ART UNIT	PAPER NUMBER

3653

DATE MAILED: 03/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/092,185

**Applicant(s)**

BEFFA, RAYMOND J.

**Examiner**

Joseph C Rodriguez

**Art Unit**

3653

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 10 February 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 2/4/05.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Double Patenting*

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-3 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-2 of U.S. Patent No. 6,147,316.

Although the conflicting claims are not identical, they are not patentably distinct from each other as the instant claims merely claim the further step of performing the enhanced reliability testing or merely describe the "enhanced" testing as further testing.

These differences are not seen as rendering the claims patentably distinct as the additional "performing" step can be regarded as implicit from the claim language of the 6,147,316 patent (See e.g., preamble claim 1 describing "IC device in need of enhanced reliability testing") and thus as obvious to one with ordinary skill in the art./

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Yabe  
(US 5,726,074).

Yabe (Fig. 5a-7b) teaches a testing method for an integrated circuit comprising storing an enhanced reliability testing flag (Fig. 7a, "Electrical Characteristics Data 3") associated with a "unique identification code" (Fig. 7a where combination of wafer ID with positional coordinates create a unique code for each chip) of each integrated circuit device of the plurality of integrated circuit devices for indicating whether each integrated circuit device requires enhanced reliability testing (col. 7, ln. 13-col. 8, ln. 10; col. 9, ln. 20-col. 10, ln. 14 teaches storing test results of specific chip that determines future quality testing of chip);

automatically reading the unique identification code of each integrated circuit device of the plurality of integrated circuit devices wherein each integrated circuit device of the plurality of integrated circuit devices forms a portion of a wafer (Fig. 6a, ID unit 3b; col. 8, ln. 1-11; col. 9, ln. 60-col. 10, ln. 4),

accessing the enhanced reliability testing flag stored for the unique identification code of each integrated circuit device of the plurality of integrated circuit devices (Id. wherein reading of "data 3" can be regarded as accessing flag);

sorting the plurality of integrated circuit devices in accordance with whether their enhanced reliability testing flag indicates they are in need of the enhanced reliability testing (Fig. 6b; col. 8, ln. 20-col. 9, ln. 18); and

performing the enhanced reliability testing for-the- each integrated circuit device of the plurality of integrated circuit devices requiring the enhanced reliability testing (Id., Fig. 6b, tester 4c).

Here, the stored information can be regarded as an "enhanced" or "further" reliability testing flag as Yabe teaches that defective chips no longer undergo testing while non-defective chips may undergo *further* sorting and testing based on narrower parameters than the original chip tester (col. 8, ln. 37-col. 9, ln. 5). That is, the use of test parameters that have been modified based on previous test results or that have been modified based on desired sorting grades can be regarded as a form of "enhanced" reliability testing as the original test parameters have been "enhanced".

### ***Conclusion***

Any references not explicitly discussed above but made of record are considered relevant to the prosecution of the instant application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph C Rodriguez whose telephone number is **703-308-8342**. The examiner can normally be reached on M-F during normal business hours (9 am – 6 pm, EST).

The **Official** fax phone number for the organization where this application or proceeding is assigned is **703-872-9326** (After-Final **703-972-9327**).

The examiner's **UNOFFICIAL Personal fax number** is **703-746-3678**.

Further, the examiner is tentatively scheduled to move in April 2005 and the contact info at the new location will be as follows:

**April 2005, Personal telephone number is 571-272-6942**

**April 2005, UNOFFICIAL Personal fax number is 571-273-6942**

Further, information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system.

Status information for published applications may be obtained from either Private PMR or Public PAIR. Status information for unpublished applications is available through Private PMR only. For more information about the PAIR system, see

<http://pair-direct.uspto.gov>

Should you have questions on access to the Private PMR system, contact the Electronic Business Center (EBC) at 866-217-9197 (Toll Free).

Alternatively, inquiries of a general nature or relating to the status of this application or proceeding can also be directed to the **Receptionist** whose telephone number is **703-308-1113**.

Signed by Examiner Joseph Rodriguez

jcr

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March 28, 2005

